Monty Choy

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San Francisco, CA

montychoy.com | linkedin.com/in/montychoy | github.com/mochoy | suild.com

Education

California Polytechnic State University, San Luis Obispo **Expected Jun. 2022 or Dec. 2022**
Bachelors of Science in Electrical Engineering *GPA: 3.90 Major, 3.71 Overall*
- President's List; Hyperloop control systems design lead, SLO Breakers, Yu-Gi-Oh Club

Experience

Apple **Jun. 2021 - Sep. 2021**
Electrical Engineering Intern - PMU Post-Silicon Validation *Cupertino, CA*
- Validated random load transient behavior & performance on multiphase buck converters
  - Developed Python script to randomly generate dynamic loads across hardware configs & PVT while adhering to overcurrent & thermal limitations of the DUT & test hardware
  - Characterized phase shedding behavior & configured distribution parameters to target phase shed timing thresholds & find potential issues in phase shed controllers
  - Automated oscilloscopes in Python to capture & process out-of-spec voltage excursions
  - Analyzed spec-violating transient response behavior & drove cross-functional FA & debug
  - Exposed limitations in test platform hardware & drove improvements for future iterations
- Implemented random load transient methodologies in dynamic aging validation of power bridges

Microsoft **Jun. 2020 - Sep. 2020**
Software Engineering Intern - Surface Duo Firmware Engineering *(Remote) Sunnyvale, CA*
- Brought-up, integrated, & developed sensor device driver on Qualcomm Snapdragon SoC
  - Deployed driver for commercialization on the Surface Duo for use by 1M+ customers
- Developed Android app, Android framework, & native libraries for modem NV configuration

Apple **(9 months) Jan. 2019 - Sep. 2019**
Hardware Engineering Intern - Apple TV Hardware Engineering *Cupertino, CA*
- Designed electrical, mechanical, & software system to characterize IR performance
- Architected, prototyped, & designed HDMI dev platform PCB. Design lead for DC-DC power, USB, & debug subsystems. Collaborated on high-speed digital (HDMI) & MCU subsystems
- Led validation, debug, & FA efforts: HDMI (CTS), PMU, SoC, SI/PI, UART, NAND, PCIe, power analysis, PDM mic hardware subsystem, & internal layer PCB failure
- Analyzed A-series SoC thermal & power performance across temperature & process corners
- Analyzed test coverage on factory line to ensure correct placement, value, etc. for every component at each test station. Increased component test coverage by over 25%

Suild **Nov. 2016 - Jul. 2020**
CEO *San Francisco, CA*
- Designed, coded, manufactured, tested, & shipped pcb-based electronics products implementing AVR MCUs, USB, UART, DC-DC converters, & PID controlled inductive loads
- Shipped 1k+ units to 10+ countries on webstore with 30k+ annual sessions & $15k+ revenue

Projects
Find more at suild.com & montychoy.com

Select-Fire Nerf Rapidstrike Kit - suild.com/shop/4 **Jun. 2019 - Jul. 2020**
- Designed PCB-based product for select-fire inductive pusher control in modified Nerf blasters
  - Manufactured, tested, shipped, & sold 300+ units to 10+ countries
- Implemented MCU, DC-DC power, PID inductive drive, and debug hardware subsystems

Technical Skills

- **Hardware Engineering:** MCUs, I2C, SPI, CAN, USB, UART, HDMI, PCB layout & design, test coverage & HW validation, computer architecture, high-speed design, system architecture
- **Power Electronics:** multiphase buck regulators, inductive MOSFET drives, LiPo batteries
- **Software Engineering:** C, C++, Python, firmware, MATLAB, system architecture
- **Hobbies:** Breakdancing, Yu-Gi-Oh, Call of Duty Mobile (Top 64 in North America)